NVMExplorer: A Framework for Cross-Stack Comparisons of Embedded Non-Volatile Memories

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ABSTRACT

Repeated off-chip memory access to DRAM drive up operating power for data-intensive applications, and SRAM technology scaling and leakage power limits the efficiency of embedded memories. Future on-chip storage will need higher density and energy efficiency, and the actively expanding field of emerging, embeddable non-volatile memory (eNVM) technologies is providing many potential candidates to satisfy this need. Each technology proposal presents distinct trade-offs in terms of density, read, write, and reliability characteristics, and we present a comprehensive framework for navigating and quantifying these design trade-offs alongside realistic system constraints and application-level impacts. This work evaluates eNVM-based storage for a range of application and system contexts including machine learning on the edge, graph analytics, and general purpose cache hierarchy, in addition to describing a freely available (`http://nvmexplorer.seas.harvard.edu/`) set of tools for application experts, system designers, and device experts to better understand, compare, and quantify the next generation of embedded memory solutions.

1. INTRODUCTION

The wide adoption of data-intensive algorithms to tackle today's computational problems introduces new challenges in designing efficient computing systems to support these applications. Hardware specialization has shown potential in supporting state-of-the-art machine learning and graph analytics algorithms across several computing platforms; however, data movement remains a major performance and energy bottleneck. As repeated memory accesses to off-chip DRAM impose an overwhelming energy cost, we need to rethink the way embedded memory systems are built in order to increase on-chip storage density and energy efficiency beyond what is currently possible with SRAM-based solutions.

In recent years, CMOS-compatible, embedded nonvolatile memory (eNVM) research has transitioned from articles and technical reports to manufacturing flows and product lines. These technologies hold incredible promise toward overcoming the memory wall problem. For example, one approach inspired by these new technologies combines the advantages of highly specialized architectures with the benefits of non-volatile memories by leveraging analog compute capabilities [26, 33, 122, 131]. On the other hand, the need for optimized on-chip storage solutions and memory innovation applies both to specialized hardware accelerators and for general-purpose CPU systems as well. More broadly, prior works have unveiled incredible potential improvements in storage density and energy efficiency by employing eNVMs across various architecture domains [56, 63, 115]. With many publications showcasing the benefits of eNVM storage technologies, it is critical for system designers to be able to explore their varying capabilities and empower efficient future on-chip storage. Unfortunately the architecture and broader research community lacks a holistic tool to identify and quantify the system and application-level implications of memory cell technologies and to make informed decisions while navigating the vast eNVM design space.

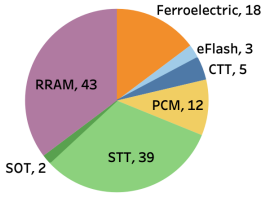

Figure 1: The number of NVM publications from VLSI, ISSCC, and IEDM 2016-2020 (cited in text) shows strong interest in RRAM and STT and an emergence of newer technologies, such as ferroelectric-based ones.

Figure 1 summarizes device and circuit conference publications relating to eNVMs from 2016 to 2020 [3, 4, 5, 6, 7, 8, 10, 12, 13, 14, 16, 18, 19, 22, 23, 24, 25, 27, 28, 29, 30, 31, 32, 34, 35, 36, 39, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 57, 58, 59, 60, 61, 62, 64, 65, 66, 67, 68, 69, 70, 71, 72, 74, 76, 77, 78, 79, 80, 81, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 111, 113, 118, 120, 121, 125, 126, 127, 128, 130, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162]. In the past five years, consistent interest in RRAM and STT was accompanied by emerging solutions with different physical properties such as FeFET-based memories. Each published example offers compelling and distinct trade-offs in terms of read and write characteristics, storage density, and reliability. In addition, the space of eNVM technologies is constantly

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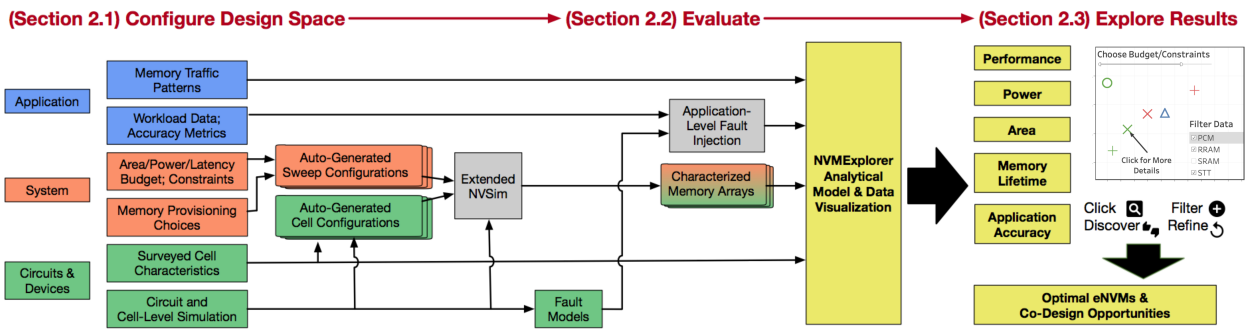

Figure 2: NVMExplorer framework overview; cross-stack design space specifications and application characteristics are evaluated in an efficient multi-stage process, then displayed in an interactive set of data visualizations to enable informed, application-aware comparisons of future on-chip storage solutions, as described in more detail in Section 2.

evolving with certain technologies moving out of fashion or into production. Given the fluidity and complexity of this design space, application experts and system designers need to be able to evaluate which cell technologies are most likely to provide better efficiency, higher storage density, or improvements on other key metrics in the context of different computing demands. Similarly, device designers and memory architects need high-level guidance to co-design their innovations toward more practical and maximally beneficial future, heterogeneous memory systems.

This work introduces NVMExplorer, an end-to-end design space exploration framework that addresses key cross-stack design questions and reveals future opportunities across eNVM technologies under realistic system-level constraints, while providing a flexible interface to empower further investigations. In this work, we describe NVMExplorer and present case studies made uniquely possible by the capabilities of NVMExplorer. In summary, NVMExplorer makes the following key contributions to the research community:

- An open-source code base including:
  - A database of eNVM cells described in recent literature (122 surveyed ISSCC, IEDM, and VLSI publications) (Section 3.1)
  - A "tentpole" methodology to summarize limits and trends across technology classes (Section 3.2)
  - Our end-to-end evaluation flow (Fig. 2)
  - Extensive source-code documentation
  - Many example configuration files and tutorial materials for cross-stack design studies
  - An interactive web-based data visualization dashboard (Section 2.3)
- A unified platform to explore the viability of eNVMs in specific application and system settings, which reveals cross-stack dependencies and optimization opportunities, in addition to reproducing and expanding previous published studies, (e.g., [115] [56]) (Section 4).
- A unified platform to perform co-design studies of application properties, system constraints, and devices in order to bridge the gap between architects and device designers for future eNVM solutions. Our example co-design studies reveal both opportunities and potential disconnects among current research efforts (Section 5).

After describing NVMExplorer (Section 2), we present a snapshot of the current eNVM landscape and extract a representative range of cell-level behavior (Section 3). Surveying recent eNVM publications reveals diverse characteristics, highlighting the challenge in identifying solutions that satisfy a broad range of application scenarios. Thus, Section 4 presents application-driven case studies using NVMExplorer to explore and analyze eNVM storage solutions for DNN inference acceleration, graph processing, and general-purpose compute. We find that each eNVM is viable in certain contexts, and the most compelling eNVM is dependent on application behavior, system constraints, and device-level choices. This finding suggests the existence of many possible architecture-device co-design opportunities, which is the focus of Section 5. Finally, we differentiate NVMExplorer from related tools (Section 6).

2. NVMExplorer

At a high level, NVMExplorer is a comprehensive design space exploration (DSE) framework integrating application-level characteristics, system constraints, and circuit and device parameters in a publicly-available, simple-to-use flow. The overall structure of NVMExplorer (Fig. 2) relies on three stages, described in more details in the following subsections:

1. A comprehensive cross-stack configuration interface to specify the design space of interest. This configuration spans the computing stack from application (blue) and system (orange) down to circuits and devices (green).

2. An evaluation engine which automatically generates configurations, simulates memory arrays, processes application behavior, computes key metrics such as perf, power, area, accuracy, and lifetime, and generates meaningful visualizations. Evaluation steps which are extensions of existing tools are shaded grey in Fig. 2.

3. An interactive, web-based visualization tool to aide discovering, filtering and refining eNVM design points.

NVMExplorer is publicly available at `http://nvmexplorer.seas.harvard.edu/`and the source code is available at `https://github.com/lpentecost/NVMExplorer`.

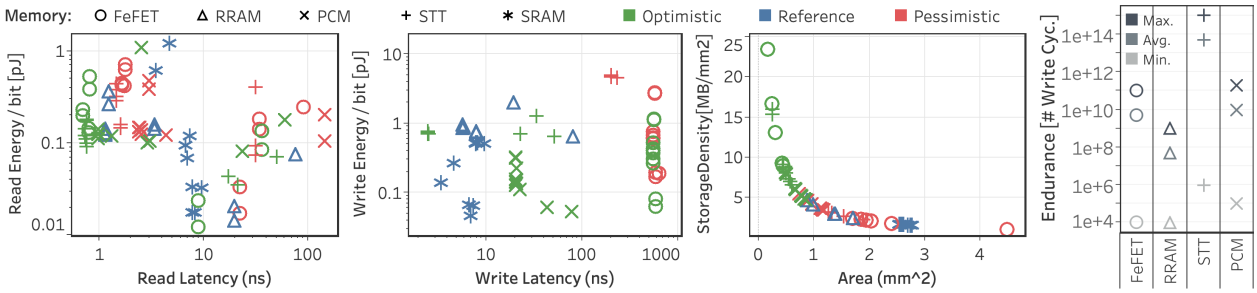

Figure 3: For fixed capacity (4MB) and under various optimization targets, array-level metrics reveal each eNVM has unique, compelling attributes. Note Pessimistic PCM write latency ($> 10\mu$s) is omitted for clarity in the write energy vs. write latency plot above.

2.1 Cross-Stack Configuration

To evaluate and compare eNVM solutions in system settings, it is not just cell or even array-level characteristics of a particular technology that matter. Rather, viable solutions depend on the area/power budget of a system and how applications running on that system interact with the memory. NVMExplorer provides a rich interface for configuring key application, system, and circuit and device parameters.

At the application level, the user inputs information about memory traffic, which may include the number of read and write operations, their proportion relative to the total number of memory accesses, and how accesses are spread out over execution time. These configuration parameters may be fixed values (e.g., characterization results of a specific workload) or provided as ranges to generate generic memory traffic patterns. Some applications may have additional demands or metrics which are tightly related to memory technology characteristics. For example, machine learning applications or approximate computing methods may trade-off relaxed accuracy for performance and energy, and NVMExplorer also provides an interface for designers to study the application interactions and implications of fault-prone eNVM solutions.

At the system level, the user has the freedom to evaluate a wide variety of memory configuration options by either setting performance, power, and area constraints and optimization goals or by choosing memory array specifications such as capacity, multi-level programming, bank configuration, and more. The circuits and devices level of the design space configuration comprises per-technology memory cell characteristics, in addition to sensing and programming circuitry choices. NVMExplorer also provides a database of eNVM cell configurations derived from ISSCC, IEDM, and VLSI publications, as described in Section 3, but it is also possible (and encouraged!) for users to extend the current NVMExplorer database with new simulation-based (*i.e.* SPICE or TCAD models), measured, or projected circuit and device properties. Once the full-stack specifications are set, NVMExplorer automatically generates configuration files, which are used as input to the evaluation engine.

2.2 Evaluation Engine

Given the auto-generated cell and system-level sweep configurations, the evaluation engine produces memory array architecture characterizations and computes application- and system-level power, performance, area, and reliability metrics. NVMExplorer combines a customized memory array simulator, an application-level fault injection tool, and an analytical model to extrapolate application-level performance metrics.

To characterize memory arrays, we rely on a customized version of NVSim, a previously validated tool to compute array-level timing, energy, and area [40]. We build on existing efforts to extend NVSim to support multi-level cells and ferroelectric-based eNVMs [115, 123]. In addition, we have modified the tool interface to ease data collection and post-processing. We introduce the capabilities of NVMExplorer in comparing eNVM candidates in Section 2.2.1. Results of cell-level and circuit-level simulations can be used to parameterize fault models and perform application-level fault injection, as described in Section 2.2.2. The analytical model takes application access counts, system settings like datawidth, and array-level results like energy/latency per access and leakage power to compute the total memory power and access latency during operation.

2.2.1 Example Array-Level Comparison

Figure 3 presents example array characterization output generated by NVMExplorer after evaluating various eNVM configurations implemented in a 22nm node. The design points are color-coded to highlight optimistic (green), pessimistic (red), or reference (blue) designs across surveyed publications per cell technology. The figure also reports the characteristics of 16nm SRAM as a comparison point. For each technology, we show array characterization under different optimization goals, which result in a variety of internal array architectures. For example, we observe a wide range for the read-energy-per-bit of an iso-capacity SRAM array. This result reflects the effect of different array optimization targets (read energy-delay product, write characteristics, area) on the internal bank configuration and periphery overhead, resulting in disparate array layouts.

This preliminary study already provides a few key takeaways. Each eNVM is able to attain read access characteristics competitive with SRAM, with the exception of an array characterized with pessimistic underlying PCM cell characteristics. However, write access characteristics vary dramatically across published eNVM examples, in addition to the range of reported endurance per technology. The tension between these properties and potential storage density (even in the absence of multi-level cell programming) indicates that array-

	SRAM	PCM	STT	SOT	RRAM	CTT	FeRAM	FeFET
Cell Area [F^2]	146	25-40	14-75	[20]	4-53	1-12		4-103
Tech. Node [nm]	7-16	28-120	22-90	[1000]	16-130	14-16	40	45
MLC	no	yes	yes	yes	yes	yes	yes	yes
Read Latency [ns]	0.5-1.5	[1-100]	1.3-19	1.4-11	3.3-2e3		14	
Write Latency [ns]	0.5-1.5	10-3e4	2-200	0.35-17	5-1e5	6e7-2.6e9	14-1e3	0.93-1.3e3
Read Energy [pJ]	1.1-2.4		0.21-1.2		1e-3		0.001	
Write Energy [pJ]	1.1-33		0.6-4.5	[0.015-8]	0.68			0.0003-0.01
Endurance [Cycles]	N/A	10^5–10^{11}	10^5–10^{15}		10^3–10^8	10^4	10^4–10^{11}	10^7-10^{11}
Retention [s]	N/A	10^8–10^{10}	10^8	10^8	10^3–10^8	10^8	10^5–10^8	

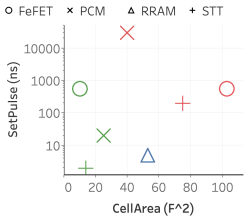

Table 1: High-level listing of memory cell technologies and ranges for key characteristics; recent publications are complemented by simulation and industry references to form technology cell definitions discussed in Section 3.1.

level comparison in isolation may guide a system designer towards sub-optimal solutions. For example, a FeFET-based memory may seem a fitting choice for high-density, read-performant storage, but we find that both performance and energy efficiency of those memories are highly shaped by application traffic patterns and underlying cell assumptions. Thus, the cross-stack nature of data exploration supported by NVMExplorer is essential in guiding system-level choices and further investigation.

2.2.2 *Fault Modeling and Reliability Studies*

In addition to characterizing memory performance, power, area, and lifetime, NVMExplorer extends previously validated efforts in application-level fault injection to provide an interface for fault modeling and reliability studies [119]. Users can provide an expected error rate or more detailed, technology-specific fault models and storage formats to perform fault injection trials on application data stored in different eNVMs. To quantify the impact on application-specific metrics of accuracy, the fault injection tool is tightly integrated with application libraries for data-intensive workloads, including PyTorch for DNNs and snap for graph processing [82, 114], as well as numpy for generic application data. As a demonstration, we perform SPICE simulation and extract fault charactieristics associated with single-level vs. multi-level cell (SLC vs. MLC) programming and sensing circuitry characteristics. In this work, we consider a subset of eNVMs, namely, RRAM, CTT, and FeFET, whose fault characteristics could be derived from existing modeling efforts [115, 123]. We use our extended fault injection framework to simulate the impact of storing workload data in SLCs vs. MLCs in Section 5.3. Armed with these additional capabilities, NVMExplorer can replicate the results of previous considerations of eNVM storage reliability [115], in addition to providing a broader platform for studying the interactions between programming choices, cell characteristics, and application accuracy.

2.3 Exploring Results & Conducting Studies

The figures in this work are snapshots from NVMExplorer's interactive web-based data visualization tool, which will be freely available at the time of publication of this work at `http://nvmexplorer.seas.harvard.edu/`. In each study, we filter and constrain evaluated results according to system optimization priorities and application use cases, as described in the text. The basic NVMExplorer data visualization dashboard presents power, performance, area, and memory lifetime results across all user-configured sweep results (e.g., many application traffic patterns, array provisioning choices, and/or eNVM cell configurations) alongside array-level metrics for a holistic design exploration experience. A user can filter results in terms of important constraints (e.g., latency or accuracy targets, power or memory area budget) and identify design points of interest. While several features of these visualizations, built using Tableau [9], are evident in the figures in this work, including dynamic filtering across plots, click-and-drag to narrow the design space, and pop-up details about results, we encourage the reader to use their imagination in how they might explore and filter the data shown in alternative ways according to their interests, questions, or confusions.

3. TECHNOLOGY LANDSCAPE

NVMExplorer provides a broad survey of published eNVM examples (Section 3.1), which can be parameterized so that systems experts can make meaningful, high-level comparisons across technologies despite different underlying trade-offs and maturity (Section 3.2). We validate this approach per-technology against fabricated memory arrays (Section 3.3).

3.1 Cell Definitions

We compile device- and array-level data across eNVM technologies including PCM, STT, SOT, RRAM, CTT, FeRAM, and FeFET-based memories. The results of this survey include read-write characteristics, endurance, and density, as summarized in Table 1 alongside SRAM properties. We source the majority of the cell-level parameters from ISSCC, IEDM, and VLSI publications and focus primarily on works from 2017-2020 to reflect the most recent range of achievable behavior per technology. Previous efforts have detailed the physical properties and limitations per technology [20], while NVMExplorer focuses on compiling sufficient cell-level details and leaning on existing technology models to provide a broad and practical database of cell definitions. While we hope these extracted cell definitions are helpful to the community in calibrating the current state-of-the-art, NVMExplorer is extensible to alternative devices as the design space continues to evolve, as demonstrated in Section 5.

The technology classes in Table 1 are at different levels of maturity. For example, SOT is a relatively recent technology, and while it boasts very impressive write speed and lower write current compared to STT, it is not yet published at advanced process nodes. We also see that endurance varies by multiple orders of magnitude across different technologies. Thus, adoption will depend on the write intensity of target applications and system dynamics, so incorporating memory lifetime estimation becomes a critical design consideration.

Grey cells in Table 1 indicate parameters unavailable in recent publications. This could be for reasons of propriety from industry fabrication or experimental constraints. However, for architects, it is important to have some concept of the possible range of values associated with these parameters. In those cases where SPICE models for a technology are available, we use simulations to fill in missing parameters. Alternatively, we consider older publications and consult with device experts to reason about cell and array parameters.

3.2 Tentpoles of the Design Space

Comparing eNVMs at varying stages of development and with varying underlying physical properties is a challenging task. The case studies in this work aim to provide high-level guidance and relative judgments about which eNVM cell technologies are worthy of further investigation under specific system and application constraints. Thus, rather than focus in on specific, physically accurate cell configurations, we aim to model the bounds of what is conceivable per eNVM technology across the full range of published recent academic work. We liken identifying and evaluating these bounds per-technology to forming the poles of a tent that encompasses the full extent of eNVM properties, so we call the extrema in terms of cell-level characteristics (i.e., smallest, lowest read energy, best retention vs. largest cell size, lowest endurance) the device-level "tentpoles". In an actively evolving technology space, this approach allows us to make meaningful classifications about which technologies are potentially adoptable solutions. These modeling choices are classified into two fixed cell configurations for applicable technologies, as summarized in Section 3.2.1 and the figure alongside Table 1. We validate that the "tentpoles" of the cell-level design space result in array-level characterization that provides coverage of published memory array properties, as discussed in Section 3.3.

3.2.1 Optimistic and Pessimistic Cell Configurations

For the technology classes most represented in our survey (Fig. 1), we compute which published example has the best-case and worst-case storage density in terms of Mb/F^2, and this data serves as the foundation of the bounds of the cell-level design space; those points which are most and least dense across recent published examples. Any critical cell-level parameters not reported with those cell definitions are assigned values (e.g., read characteristics and programming settings) using the best (lowest power, highest efficiency) or worst (highest power, lowest efficiency) value per metric across all other recent publications with sufficient supporting data. These best-case and worst-case technologies per class form the tentpoles of the underlying cell design space, and we label these fixed cell definitions as "optimistic" or "pessimistic" accordingly. For the purposes of the case studies presented in Sections 4 and 5, all array- and application-level results are produced using these fixed underlying optimistic and pessimistic cell properties, though we note that a user of NVMExplorer can draw either on these constructed, bounding example cells or on the full database of surveyed configurations, or on fully customized definitions with respect to cell size, access properties, and operating conditions (e.g.,read/write voltage, temperature). Corresponding fault

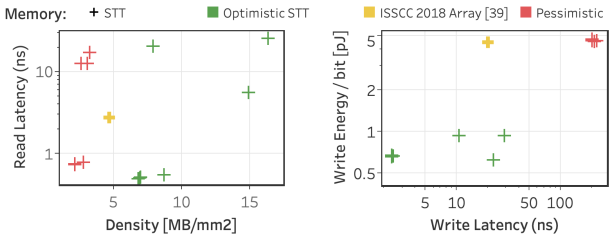

Figure 4: "Tentpole" STT vs. published array data shows coverage of the space across critical metrics.

models and error rates for reliability studies are extracted after optimistic vs. pessimistic cell-level properties are fixed, as discussed in one of the presented case studies (Section 5.3).

This approach helpful for many reasons: for one, these extremes help us answer exploratory questions about what we will likely see in the near future; secondly, comparing the best-case of one technology to the worst-case of another can help gauge less mature technologies against more mature reference points; thirdly, if such optimistic configurations are untenable or even pessimistic configurations are attractive in a specific system setting, we can build confidence for further exploration and more detailed modeling efforts without implementing and attempting to meaningfully compare many many cell definitions with insufficient data. A limitation of this methodology is that inherent trade-offs between certain parameters for a technology may not be linked (e.g., area, latency, and retention for STT); however, this amalgam of cell properties represent the full spectrum of achievable characteristics per technology, rather than specific fabricated results. As a point of additional comparison, the results shown in the following studies include a reference cell configuration for RRAM as a relatively mature eNVM, with parameters derived from a specific industry result [31]. The resulting optimistic, pessimistic, and reference cell size and write pulse are shown to the right of Table 1.

3.3 Validation

Our array-level area, energy, and latency characterizations rely on the previously-validated procedures of NVSim to extrapolate cell-level configurations and array design constraints to optimized memory layouts and properties [40]. However, in employing our "tentpole" approach, it is critical that we verify that array-level results using our optimistic and pessimistic underlying cell characteristics fully cover and match expectations of existing fabricated eNVM solutions.

Whenever possible, we select publications with array-level characterizations for a given technology, and compare those results to iso-capacity memory arrays modeled through our "tentpole" approach. Figure 4 shows an example of such an exercise. We compare a 1MB STT-RAM array published at ISSCC in 2018 to optimistic and pessimistic STT design points produced by NVMExplorer. Here, we note that our tentpole results effectively represent the range of actual array properties by producing metrics that are both higher and lower, but similar in magnitude, to the reference STT-RAM array. The studies presented in this work consider only validated configurations for which we were able to either com-

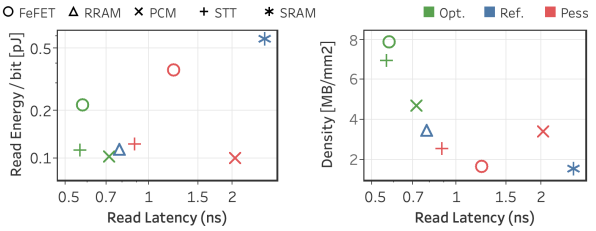

Figure 5: Read characteristics and storage density for 2MB arrays, provisioned for replacement of on-chip SRAM in NVDLA.

plete this validation exercise or run SPICE-level simulations. It is worth noting that NVMExplorer is set up to evaluate all technologies in Table 1 following more rigorous validation or future publications. System validation and application characteristics are derived from existing, state-of-the-art references, as addressed in each study in Section 4.

4. APPLICATION-DRIVEN CASE STUDIES

We now present three case studies that highlight different ways NVMExplorer can search design spaces in order to identify benefits and limitations of the diverse range of eNVM storage solutions. Each scenario presents unique optimization goals and system priorities and, in each case, we compare how each eNVM's power, performance, and area fairs relative to similarly-provisioned SRAM or DRAM in a baseline system.

4.1 DNN Inference Accelerator

Prior studies have demonstrated the potential benefits of eNVM storage for Deep Neural Network (DNN) inference accelerators [37, 115, 146], albeit with limited scope in terms of eNVM technologies and cross-stack parameters considered. NVMExplorer empowers researchers to approach a broader set of questions that compare eNVMs in different storage scenarios (e.g., limited to weights vs. storage of DNN parameters and intermediate results) and system constraints (e.g., strict area budget, or power budget). In this work, we consider two distinct use cases for a DNN inference accelerator: continuous operation, as in image processing per frame of a streamed video input, and intermittent operation, where the system is woken up per inference task and can leverage the non-volatility of eNVM by retaining DNN parameters on-chip in power-off state between inferences.

4.1.1 Continuous Operation

We consider the commonly-used and well-studied NVDLA [129] as a base computing platform and compare its 2MB SRAM with iso-capacity eNVMs. We use the NVDLA performance model [110] to extract realistic memory access patterns and bandwidth requirements of the on-chip buffer. More specifically, we evaluate the power and performance of accesses to on-chip memory storing ResNet26 weights for single-task image classification using the ImageNet dataset vs. multi-task image processing, comprising object detection, tracking, and classification, at a consistent frame rate of 60 frames-per-second, as is typical for HD video. We additionally consider the impact of storing activations in eNVM, but this ostensibly ignores endurance limitations.

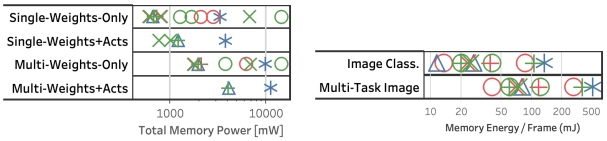

Figure 6: The most energy-efficient eNVM varies under different DNN inference use cases, such as continuous (left, operating power) vs. intermittent (right, reporting energy per input image frame); these results exclude eNVM solutions that are unable to meet application latency and accuracy targets.

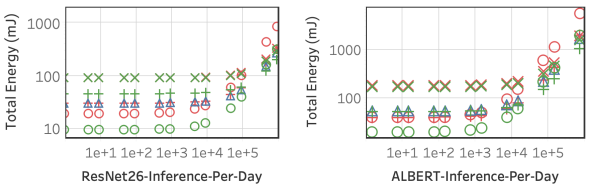

Figure 7: The eNVM storage solution (iso-capacity arrays provisioned per task, optimized for ReadEDP) that minimizes total memory energy consumption varies according to system wake-up frequency and DNN inference task; All solutions shown maintain application accuracy and a $< 1s$ latency per inference.

First, we observe the read and storage density characteristics for 2MB arrays using the cell-level tentpoles of several promising eNVM technology classes, FeFET, STT, PCM, and RRAM, as shown in Figure 5 compared with SRAM. Notice that read energy effectively divides arrays into two tiers. STT, PCM, and RRAM offer lower read energies across a wide range of read latency that still outperform SRAM. In contrast, FeFET-based eNVMs suffer from higher read energies, but notice that an optimistic FeFET offers the highest storage density with low latency. At similar low latency, optimistic STT offers 6× higher density over SRAM. PCM and RRAM outperform SRAM in terms of both read latency and storage density. While such comparative insights can readily be extracted from this pair of plots, there are other important dimensions to also consider, and NVMExplorer facilitates more comprehensive analyses that consider the impact of application priorities and system-level use cases on eNVM design decisions.

Considering more dimensions of the design space, Figure 6 (left) summarizes total operating power (both dynamic access and leakage power) for the 2MB memory arrays characterized in Figure 5 and accessed according to continuous traffic patterns of different ResNet model deployment scenarios, i.e., single- vs. multi-task and weights-only vs. storing both weights and activations. These results exclude eNVM candidates that cannot support 60 FPS operation nor maintain DNN accuracy targets. Recall NVMExplorer includes fault injection wherein high eNVM fault rates can degrade model accuracy to unacceptable levels. While not explicitly shown here, NVMExplorer considers numerous additional interactions for users to probe, explore, and build intuition. For example, while total memory power increases as the number of accesses per frame increases to compute multiple

tasks, the ratio of read-to-write traffic stays roughly the same. Hence, the relative power of eNVM arrays also remains similar. In particular, PCM, RRAM, and STT all offer over 4× reduction in total memory power over SRAM. One important reason for this is that SRAM leakage power will dominate compared to eNVM solutions, even under high traffic. Of the energy-efficient solutions, STT offers best performance (lowest application latency per frame). In contrast, optimistic FeFET offers higher storage density while maintaining 60FPS and a 1.5-3× power advantage over SRAM.

4.1.2 *Intermittent Operation*

Let us now consider eNVM storage for two additional use cases that alter system-level optimization goals and corresponding eNVM selection, further highlighting the flexibility and ease of exploration the NVMExplorer framework offers. A major advantage of storing DNN weights in eNVMs is that non-volatility supports intermittent operation that powers off the accelerator between inferences. Using SRAMs would either consume leakage power to keep the weights memory powered on or consume power to restore the weights from off-chip memory, e.g., by incurring a latency and energy penalty by fetching from DRAM. In this use case, we provision monolithic eNVM storage to hold all DNN weights (e.g., 8MB for image tasks and up to 32MB for Natural Language Processing (NLP) tasks). For image processing, all weight memory accesses are to eNVM, eliminating the otherwise-required wake-up latency and power associated with loading parameters into on-chip SRAM, in addition to reducing distance between compute system and higher-capacity memory.

Figure 6 (right) compares the resulting memory-energy-per-inference across eNVMs for both single-task image classification and multi-task image processing, as determined by the total number of accesses to retrieve all DNN weights over the course of processing one input frame. The lowest-energy technology choice differs between the single vs. multi-task inference and, perhaps more interesting, both are eNVM candidates with *lower* storage density (RRAM and pessimistic FeFET), as opposed to the highest density options (STT and optimistic FeFET), which hints at a cross-stack prioritization of read performance as opposed to cell size reduction, as probed further in Sec. 5.2. We repeat this study for single task vs. multi-task natural language processing using the ALBERT network, a relatively small-footprint, high-accuracy, transformer-based DNN [75].

To further study this result, we dig into the implications of intermittent operation and compare the total energy versus the number of inferences per day, showing a continuum of wake-up frequency that may arise (e.g., deployed solar-powered agricultural sensors or satellites, or a voice-enabled assistant executing NLP tasks on wake-up). The left plot of Figure 7 shows total memory energy as a function of inferences per day for image classification. Here, total memory energy is presented as a proxy for device battery life. From the figure, we observe that when the number of inferences per day is sufficiently low (less than 1e5), optimistic FeFET yields the lowest energy. At higher wake-up frequency, optimistic STTs take over because of the relatively lower energy-per-access. Figure 7 (right) investigates the impact on an NLP workload. While results are similar, optimistic STT emerges as the best technology at lower inference rates (as compared to image classification), because ALBERT requires more computational power per inference than ResNet26.

Table 2 summarizes the preferred eNVM technology across different use cases and tasks, with "Opt. eNVM" indicating the preferred choice under optimistic underlying cell characteristics and "Alt. eNVM" indicating the preferred technology assuming pessimistic assumptions and reference points, and table entries for intermittent operation are selected at a fixed wake-up rate.

Across a range of device wake-up frequencies and per-wake-up compute patterns, we observe that several eNVMs become compelling, and the preferred NVM choice for further investigation varies depending on both of these factors.

Use Case	Inference Task	Data Storage	Priority	Opt. eNVM	Alt. eNVM
Continuous (60IPS)	Single-Task Image Classification	Weights Only	Low Power	PCM	PCM
			High Density	FeFET	CTT
		Weights + Acts	Low Power	PCM	RRAM
			High Density	STT	RRAM
	Multi-Task Image Processing	Weights Only	Low Power	PCM	RRAM
			High Density	FeFET	CTT
		Weights + Acts	Low Power	STT	RRAM
			High Density	STT	RRAM
Intermittent (1IPS)	Single-Task Image Classification	Weights Only	Low Energy/Inf	RRAM	RRAM
			High Density	FeFET	CTT
	Multi-Task Image Processing	Weights Only	Low Energy/Inf	FeFET	FeFET
			High Density	FeFET	CTT
	Sentence Classification (ALBERT)	Embeddings Only	Low Energy/Inf	RRAM	RRAM
			High Density	FeFET	CTT
		All Weights	Low Energy/Inf	STT	RRAM
			High Density	FeFET	CTT
	Multi-Task NLP (ALBERT)	All Weights	Low Energy/Inf	STT	RRAM
			High Density	FeFET	CTT

Table 2: Summary of preferred eNVM under varying DNN use case, task, storage strategy, and optimization priority.

4.2 Enabling Efficient Graph Processing

Our second case study explores the potential benefits of using eNVMs for graph processing, which imposes an entirely different set of constraints in terms of memory read and write characteristics. Graph processing comprises many read-dominated tasks with less predictable data reuse than DNNs (e.g., search kernels), but still involves write traffic and, overall, is incredibly data-intensive in terms of memory bandwidth and capacity. As an initial exploration of compatibility and viability between graph processing workloads and eNVM storage solutions, we consider the total power and resulting memory lifetime per technology under generic traffic patterns covering the range of read and write bandwidths for critical graph tasks, as described in previous workload characterization efforts [11]. As a proof of concept in a specific system, we additionally evaluate eNVM storage solutions under access patterns for benchmarks executed on a domain-specific accelerator [55].

4.2.1 *Analysis for generic traffic patterns*

We consider different memories experiencing a range of generic traffic patterns representing graph processing kernels (i.e., read access rates from 1-10GB/s and write access rates from 1-100MB/s) [11]. NVMExplorer provides a wide array of critical metrics to compare and user-configurable visualizations to extract important trends and limitations. For example, in Figure 8, we choose to display total memory power against read traffic, as number of read accesses becomes a dominant factor in total power for read-dominated workloads, and total

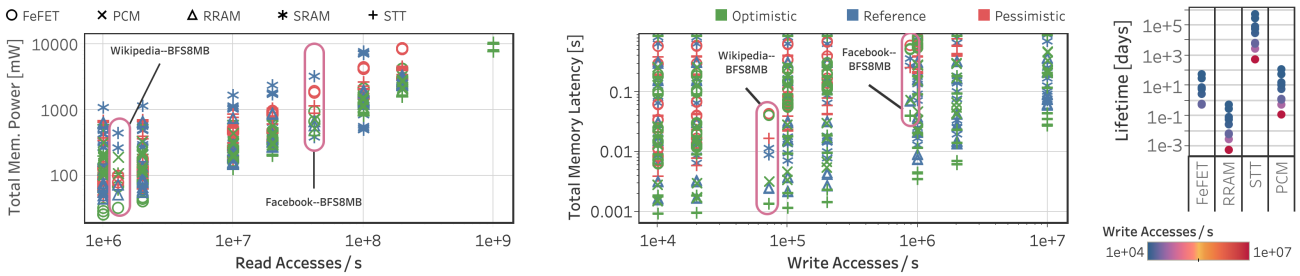

Figure 8: Memory power, latency, and projected lifetime for generic traffic patterns encompassing graph processing demands, including specific graph kernels as labeled. The lowest power solution depends on the expected read traffic. FeFET solutions fail to match SRAM performance. STT provides superior performance and memory lifetime.

memory latency against write traffic, as overall performance for several eNVMs is strongly determined by write traffic.

As shown by Figure 8, left, total memory power generally increases with read access rate and the lowest power solution depends on the application traffic load. For applications that exhibit fewer than 10^7 read accesses per second, optimistic FeFET is a clear winner, while pessimistic FeFET and RRAM are next best candidates. On the other hand, for higher rates of read traffic (e.g., $> 10^8$), optimistic STT is best. For mid-range read access rates, PCM and RRAM are also viable solutions sometimes offering the lowest power solution. However, this relationship alone does not dictate memory technology choice. A slightly different and more consistent story emerges when we analyze the impact of different eNVMs on overall memory latency (both read and write) versus write access rates, shown by the middle plot of Figure 8. While there is a clear preference for optimistic STT, RRAM and optimistic PCM are also worth considering. In contrast, most pessimistic eNVM technologies and all FeFET-based solutions are significantly inferior, even failing to match SRAM performance for many traffic patterns.

When we additionally consider projected memory lifetime, STT emerges the clear winner overall. Note that the right chart of Figure 8 plots the memory lifetime assuming continuous operation at a particular write access rate. Hence, the highest write traffic always yields the lowest lifetime. While RRAM seemed promising based on performance and power, it has the worst endurance and lowest lifetimes.

4.2.2 *Analysis for domain-specific systems*

In addition to relying on generic traffic patterns to represent the full range of expected traffic loads of graph processing, NVMExplorer can also be leveraged to answer a more specific design question: For performance targets and traffic patterns to a specific storage resource in a graph processing accelerator system, which eNVMs offer compelling characteristics that warrant further investigation? To this end, Figure 8 also includes points, identified in pink, corresponding to memory traffic to run breadth-first search on two different social network graphs (Wikipedia and Facebook) [82]. Traffic patterns are extracted from throughput and accesses reported for the compute stream of a domain-specific graph processing accelerator utilizing an 8MB eDRAM scratchpad [55]. In the baseline system, about 90% of the energy is spent on the eDRAM scratchpad (not including DRAM controller energy), with an operating power of at least 3.1W at the 32nm process technology node as reported from Cacti [55,112]. We analyze the benefits of replacing the 8MB eDRAM scratchpad with an iso-capacity eNVM array provisioned to meet the cited latency target (1.5ns).

If we exclude RRAM due to low lifetime projections, FeFET, PCM, and STT all offer significantly lower memory power (about 2-10× lower than SRAM) and even pessimistic STT offers consistent performance. These observations, based on a realistic graph processing use case extracted from prior work, are consistent with the results generated using generic traffic patterns. Again, optimal technology choice depends on system-level optimization goals, and NVMExplorer provides critical insights in the presence or absence of a specific system solution and simulation results.

If the high-level goal is to maximize storage density, FeFET is highly attractive, but severely limited by poor write latency (unable to meet application latency expectations under the higher range of traffic patterns). Rather than prematurely eliminating FeFET, designers can leverage NVMExplorer to study the impact of relaxing or adapting application targets or to explore co-design solutions that target improvements to the underlying technology (Sec. 5.1) or architecture (Sec. 5.4).

4.3 Non-Volatile LLC Solutions

Improved density and energy efficiency could revolutionize general-purpose on-chip storage, and recent efforts have endeavored to replace high-performance memories, like caches, with eNVM-based alternatives [56,63,73]. However, caches must handle a large volume of writes depending on the application, so the achievable write latency and endurance per eNVM comes to the forefront of design considerations.

In this study, we consider the last-level cache (LLC) of a high-performance desktop processor, similar to Intel's 14nm, 8-core Skylake. The memory hierarchy includes a private 32 KiB L1I$; a private 32 KiB L1D$; a private 512 KiB L2$ (non-inclusive, write-back); and a shared ring 16MiB L3$ with 64 B line, 16 ways (inclusive and write-back). The system includes DRAM with 2 channels, 8 B/cycle/channel, 42cycles + 51 ns latency. Representative application behavior comes from SPECrate CPU2017 (integer and floating point), and we warm-up the cache for 500M instructions and simulate for 1-billion instructions in detail using the Sniper simulator [15, 17]. This provides application modeling data for a 16MB LLC (e.g., reads, writes, execution time per benchmark) that are inputs to NVMExplorer (see Section 2.1).

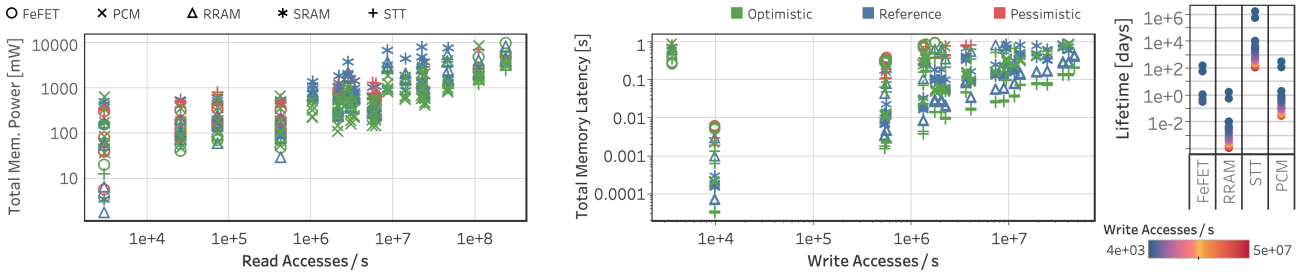

Figure 9: Memory operating power, latency, and projected lifetime under continuous operation across SPEC benchmark traffic to a 16MB LLC shows preferred eNVM depends on traffic demands and optimization goal. All solutions shown meet per-benchmark read/write demands. For high-traffic benchmarks, STT provides lowest power, lowest latency, and longest projected lifetime.

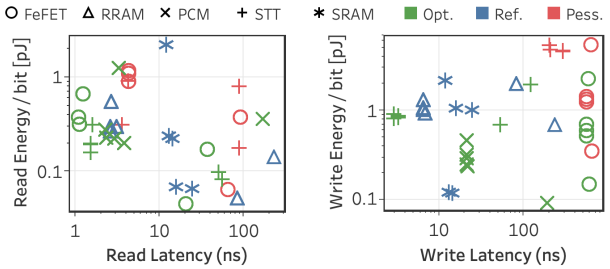

Figure 10: Array access characteristics in isolation for consideration of replacing (iso-capacity) a 16MB LLC.

First we focus on the array characteristics of the different memory technologies in isolation, as shown in Figure 10. From the left plot, we note a competetive range of read energy and read latency does not reveal a clear winner. For example, if read energy per access is highest priority, FeFET, RRAM or even SRAM offer array configurations that trade access latency for energy efficient, while STT and optimistic FeFET offer pareto-optimal read characteristics. For writes (Figure 10, right), a PCM-based last level cache appears to minimize energy per access. On the other hand, only STT and RRAM are able to beat SRAM write latency. Again, we find array characteristics in isolation do not offer sufficient guidance to choose the best eNVM for LLC, and NVMExplorer allows us to go further.

Figure 9 shows the resulting power, performance, and lifetime when using different eNVMs as LLC and assuming memory traffic from SPEC2017 benchmarks. The leftmost figure shows total memory power versus read access rate, where each column of points corresponds to a particular benchmark traffic pattern. We again see that the lowest power eNVM solution depends on the traffic pattern. In broad terms, RRAM and FeFET fair better for lower read access rates while PCM is better for higher rates until STT emerges best for the highest rates. In terms of memory access latency with respect to write access rates, STT is usually the best choice, though arrays unable to meet application bandwidth are excluded. Lastly, the rightmost figure compares lifetimes across the eNVM technologies for a range of write access rates. Again, STT offers the best longevity on average. However, PCM and FeFET may warrant consideration for read-dominated workloads. RRAM, on the other hand, does not appear viable as an LLC.

5. CO-DESIGN OPPORTUNITIES

Exploration of the design space in Section 4 shows that no single eNVM technology is best. Rather, technology choice depends on the application and system-level targets. This also means there are ample co-design opportunities across the computing stack – from devices to architecture. By contextualizing and evaluating high-level implications of cell-level innovations as they emerge, one can identify what system-level opportunities are unlocked by that change.

5.1 Alternative FeFET fabrication choices unlock performant solutions for graph processing

Previous FeFET-based device characterization and modeling efforts have exhibited write pulses on the order of $100ns$-$1\mu s$. However, alternative FeFET fabrication strategies in early development stages, such as back-gated FeFETs [124], offer compelling potential advancements in write latency ($10ns$ programming pulse) and projected endurance (10^{12}). Section 4.2 noted that the primary limition of FeFETs in the context of graph processing was an inability to meet the application latency targets under higher write traffic. Thus, using the underlying cell properties of back-gated FeFETs reported in [124], we can rapidly re-examine the viability of FeFET-based memory and probe whether this change could make a difference in the viability of FeFET-based memory for graph processing.

Figure 11 shows the total memory power and total memory latency of an 8MB memory array of back-gated FeFETs (in yellow) compared to using previous FeFET standards (red, green) and SRAM (blue). We examine these metrics under a range of read and write traffic patterns which are inclusive of the graph benchmarks described in Section 4.2 and the SPEC benchmarks used in Section 4.3, but here showing access patterns for an 8MB capacity LLC. The underlying array-level characterization is shown in Figure 11, right. From the array characterization, we observe that the back-gated FeFETs show a slight increase in read energy per access and slight decrease in storage density compared to prior state-of-the-art cells. However, we observe that they enable comparable application latency to SRAM across a wide range of write traffic where previous FeFET versions fall short. Furthermore, back-gated FeFETs results in the lowest operating power over most of the range of read accesses per second, including for the example graph processing benchmark, Wikipedia–BFS8MB.

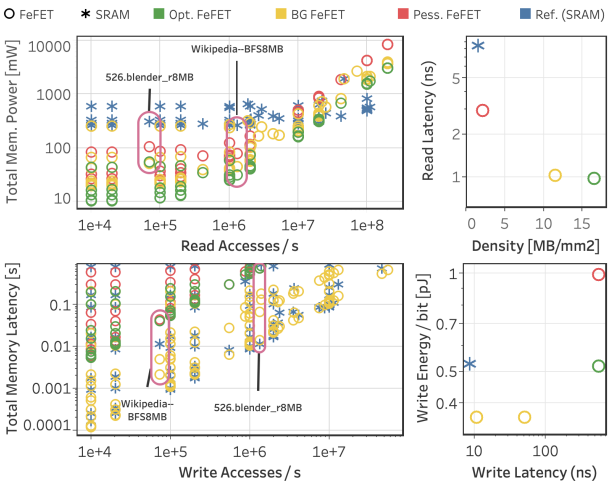

Figure 11: Back-gated (BG) FeFETs provide the high density and low operating power for example graph processing benchmarks with SRAM-comparable performance and begin to close the performance gap between non-BG FeFET and other memory technologies across SPEC2017 benchmarks.

Based on these observations, we can conclude that back-gated FeFET memory may close the performance gap between non-BG FeFET and other memory technologies (including SRAM) and unlock additional application domains. NVMExplorer's ability both to quickly and efficiently gauge the impact of cell-level innovations and to match emerging device designs to compelling use cases can enable productive future co-design collaborations. This feedback loop is mutually beneficial in providing direct motivation for further device development and encouraging system designers to integrate more energy-efficient, highly dense on-chip memory.

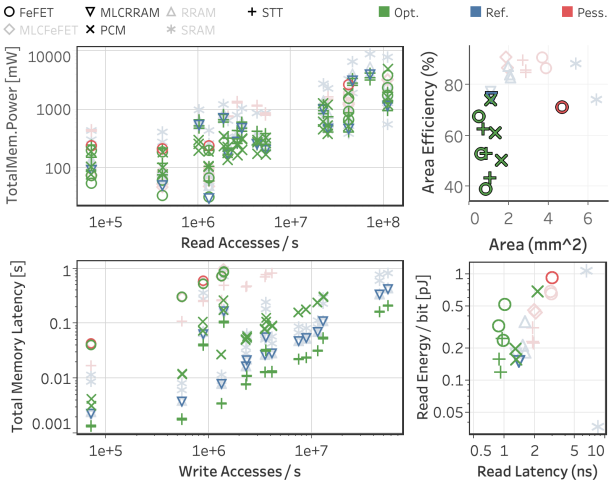

Figure 12: Results for 8MB arrays are filtered according to a maximum area efficiency bound in the top right plot. Arrays with lower area efficiency are highlighted across all views and tend to result in low memory latency across many traffic scenarios.

5.2 Trade area efficiency for performance

One theme we can highlight across the architecture-driven case studies from Section 4 is that the subset of characterized results that exhibit lower area efficiency (i.e., internal array architectures that do less amortization of periphery and sensing overhead) also tend to result in lower total memory latency across many traffic scenarios. This is perhaps counter-intuitive given the effort spent in the devices community to manufacture very small cell sizes. We also note that in Figure 12, where such design points are highlighted across the plots, that slight advantages in terms of energy-per-access (e.g., Opt. STT and PCM compared to FeFET) tend to correlate to large total power advantages in high-traffic scenarios. As such, pointing out to device designers the greater relative impact of reduced energy per access rather than decreased cell size could usher in a more productive, product-ready set of eNVM technologies. Additionally, we observe that reducing energy per write access for STT and RRAM would drastically improve their relative power advantage for data-intensive applications, even at a cost of relatively lower area efficiency or storage density.

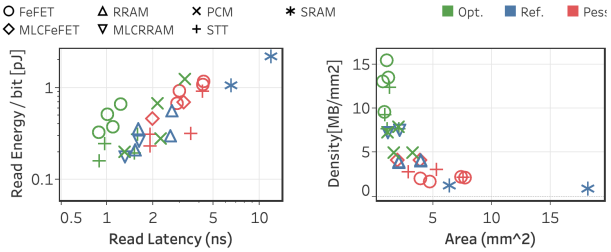

Figure 13: When we consider multi-level cell (MLC) storage and filter out 8-16MB capacity arrays that don't provide acceptable ResNet18 inference accuracy after fault injection trials, we note MLC RRAM offers denser, more performant memory than SLC RRAM while meeting application accuracy, while MLC FeFET is only sufficiently reliable for larger cell sizes (red points).

5.3 Advantages of multi-level programming vary among eNVMs

While programming multiple bits per memory cell is an important strategy for increasing storage density across many eNVMs, previous work has revealed that MLC eNVMs often exhibit significantly higher fault rates that must be carefully considered in conjunction with application resilience [115]. NVMExplorer enables efficient and broad probing of reliability vs. storage density by providing an application-agnostic fault injection tool and templates for technology-specific fault modes, as discussed in Section 2.2.2. To demonstrate, we evaluate the impact of density on application accuracy for ResNet18 weights (image classification) under storage in SLC vs. 2-bit MLC across multiple technologies which provide MLC capabilities and for which there exists sufficient cell and circuit level modeling to produce detailed fault models. The density vs. reliability trade-off is distinct for each technology. For example, Figure 13 displays 8MB and 16MB characterized arrays, including 2-bit MLC RRAM and 2-bit

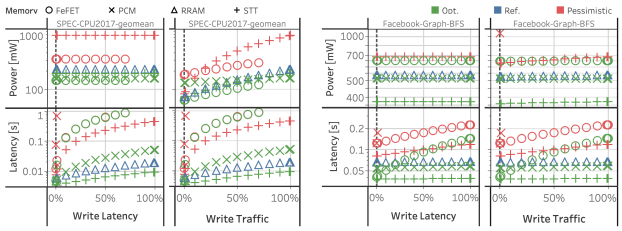

Figure 14: Masking write latency or reducing write traffic via introduction of a write caching scheme could enable a broader set of eNVM technologies.

MLC FeFET, filtered such that only those arrays meeting application latency requirements and maintaining image classification accuracy are included. Note that these results replicate previous efforts that indicate that image classification inference is robust to 2-bit MLC RRAM storage (we also verified this for CTT-based memories with fault modeling details provided in [38, 115]), while we show that MLC FeFET devices only exhibit acceptable accuracy for larger cell sizes. This is because smaller FeFETs are more difficult to program reliably due to device-to-device variation [123]. Portions of NVMExplorer were leveraged to quantify cell- and circuit-level trade-offs specific to MLC FeFETs in greater depth to determine optimal cell provisioning and writing schemes for target applications [123].

5.4 Write buffering changes the performance landscape

In conjunction with technology innovations to reduce write latency, adoption of a wider set of eNVMs in general-purpose computing contexts could be made possible by employing existing architectural techniques to mask poor write characteristics. For example, in an effort to extend memory lifetime and mask the performance impact of write access, a more performant technology (e.g., SRAM, or STT) could be employed as a write-buffer. Rather than employ a costly and engineering-intensive cycle-accurate simulator to gauge the impact of provisioning a write buffer, NVMExplorer enables an analytical study under user-specified traffic patterns to narrow the space of eNVMs worthy of further simulation and design effort. This approach answers high-level questions regarding whether write-buffering could make a difference in making additional eNVMs viable for applications with significant write traffic, and, if so, how much benefit would need to be extracted using the write buffer?

For illustrative purposes, we consider a simple write cache that would hold write requests to the eNVM, write back to eNVM when the buffer is full, and allow in-place updates in the case of multiple writes to the same address before an update to eNVM. Figure 14 shows the results for this study for SPEC2017 and Facebook-Graph-BFS.

Just buffering the writes will mask the effective write latency experienced by the system, while a write cache that allows updates could additionally reduce traffic and extend lifetime. In particular, we look at the effects of masking write latency and reducing write traffic on total memory latency and power. We observe that for Facebook-Graph-BFS, if the write traffic load is reduced by at least half, FeFET emerges as a performant option, while STT remains the lowest power solution for this particularly high-traffic workload. STT and RRAM are still the optimal technology choices for SPEC2017 in terms of performance, but write-buffering could empower FeFETs as a lower-power alternative if latency could be masked or write traffic to the eNVM could be reduced by at least 25%.

6. RELATED WORK

Previous work in evaluating eNVM technologies can be characterized by either focusing on device- and array-level evaluations, or providing in-depth cross-stack evaluations based on particular combinations of eNVM devices and application targets. In Table 3, we codify the key differences between NVMExplorer and related works. Survey works such as the Stanford Memory Trends [2] maintain a list of key eNVM parameters, like storage capacity and write energy, while previously validated array-level characterization tools, such as NVSim [40], characterize timing, energy, and area of eNVM-based memory structures. DESTINY [117] modifies NVSim to evaluate 3D integration and could be similarly extended and used as a back-end characterization tool for NVMExplorer.

To evaluate eNVMs in a system setting, prior work typically integrates NVSim with a system simulator. DeepNVM++ [63] enables design-space exploration of MRAM-based technologies in the context of GPU cache for DNNs using GPGPUSim. NVMain [116] enables evaluation of eNVM-based main memory using gem5. NeuroSim+ [21] focuses on evaluation of processing-in-memory for DNN inference and training using eNVMs. Existing works such as these provide limited or otherwise domain-specific design space exploration frameworks.

In contrast, NVMExplorer offers more breadth by including application-, system-, and device-level considerations, and accommodating a wider range of devices without requiring a separate system simulator. Additionally, NVMExplorer offers a broad range of evaluations, including fault modeling and reliability studies. It is built for ease of navigation and fluidity, and it exposes the unique cross-stack trade-offs among application characteristics, system constraints, and circuit and device level innovations in a user-friendly configuration interface and companion data visualization interface.

		Tech. Surveys		Array Simulators		Arch-Specific Frameworks			This Work
		IRDS [1]	Mem. Trends [2]	NVSim [40]	DESTINY [117]	Neuro-Sim+ [21]	NVMain [116]	Deep-NVM++ [63]	**NVMExplorer**
NVM	RRAM	✓	✓	✓	✓	✓			✓
	STT		✓	✓	✓	✓	✓	✓	✓
	SOT		✓					✓	✓
	PCM		✓	✓	✓	✓	✓		✓
	CTT								✓
	FeRAM	✓	✓						✓
	FeFET		✓			✓			✓
Circuits	MLC					✓			✓
	Fault Modeling					✓			✓
Architectural Simulator / Use Case						Focus on PIM for DNNs	gem5	GPGPU-sim for DNNs	Analytical; CPU, GPU, accelerator included
App-Aware Evaluation	Accuracy					✓			✓
	Memory Lifetime						✓		✓
	Operating Power					✓	✓	✓	✓
	Latency					✓	✓	✓	✓

Table 3: NVMExplorer leverages existing efforts by extending NVSim, while providing novel cross-stack DSE and guidance with more breadth than previous works.

By integrating these components, NVMExplorer serves an additional purpose of providing a platform for architects and device designers to perform co-design evaluations required for the advancement of technologically-heterogeneous memory systems.

7. CONCLUSION

Next-generation on-chip memory will need to push the boundaries of efficiency and density, and a diverse set of embedded non-volatile memory (eNVM) technologies have compelling characteristics to address these limitations. NVMExplorer provides architects the flexibility to explore and compare these storage solutions under realistic constraints. As a demonstration of NVMExplorer's capabilities, we evaluate and compare eNVM solutions for DNN inference tasks, graph processing, and general-purpose computing scenarios. We find that depending on system optimization goals and application properties, each eNVM emerges as a compelling candidate in at least one critical computing context, and there are key limiting characteristics both at the application level and the cell level. This finding suggests the existence of cross-stack optimization opportunities, and NVMExplorer empowers efficient and informative co-design studies such as alternative FeFET fabrication strategies to improve write access and enable support for graph processing or incorporating write caching to change the relative performance and power benefits of various eNVM solutions. NVMExplorer is open source, with interactive data visualizations freely available online, which we hope will unlock the potential of eNVMs in a broad range of systems.

Acknowledgements

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