Power Delivery Design and Optimization in 3D Integrated Circuits

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Motivation

- Three dimensional (3D) integrated circuits (ICs) promise high bandwidth, low latency, low device power, and small form factor.
- Dies from disparate technologies (analog, digital, mixed signals, sensors, antenna, and power storage) as well as from different technology nodes (65nm, 45nm etc) can be stacked to form circuitry with three dimensional stacked dies.
- While robust on-chip power delivery for planar 2D ICs is considered one of the ITRS scaling challenges, power delivery is even more difficult for 3D ICs due to increased power density (devices per square area) and package asymmetry.

Part I: Comparative Study of 2D and 3D IC

In this section of my thesis I study several 3D power delivery configurations with the goal of understanding the major factors that impact 3D power delivery network (PDN) quality. These factors are:
- TSV size and spacing.
- C4 package bump spacing.
- Combination of dedicated and shared power delivery.
- Co-axial TSV to improve power quality, reduce blockages, and signal overlap.

Part II: On-chip Power Delivery Using Carbon nanotubes

CNTs have emerged as a promising building block for future VLSI technologies due to low resistivity, high thermal conductivity, and electromigration. I analyze the electrical and thermal impact of using CNT for routing the power delivery network. I propose growing CNT on a separate silicon die (an interposer) and integrating it with the chip through bonding. I utilize a practical and realistic model for CNT bundles incorporating a mixture of single-walled and multi-walled CNTs and include metallic and semiconducting CNTs with diameter variations.

Part III: Optimization of Substrate Area Dedicated to PDN TSVs

The third part of my thesis focuses on the optimization of silicon area dedicated to TSVs for power delivery. TSVs can be used to route inter-die signals, deliver power to each die, and extract heat from the dies away from the heat sink. TSV's pass through the silicon substrate and occupy valuable silicon real estate introducing blockage for the devices and interconnects.

References


Figures:

- Maximum (a) and average (b) IR drop for Cu and CNT based on-chip power grid
- TSV Size vs. Granularity of TSV
- Thermal Analysis of Cu and CNT Power Grid

Tables:

<table>
<thead>
<tr>
<th>Diameter Size (µm)</th>
<th>Cu TSVs</th>
<th>CNT TSVs</th>
<th>Cu TSVs</th>
<th>CNT TSVs</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 x 2.5 m</td>
<td>0.70</td>
<td>0.90</td>
<td>0.85</td>
<td>1.00</td>
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<tr>
<td>5.0 x 5.0 m</td>
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<td>1.15</td>
<td>1.10</td>
<td>1.30</td>
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<tr>
<td>7.5 x 7.5 m</td>
<td>1.20</td>
<td>1.45</td>
<td>1.25</td>
<td>1.50</td>
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</table>

For signal TSVs, the TSV induced substrate noise is an important factor to calculate the area of these blockages. For power delivery network, however, it is more important to optimize the total number of TSVs and the cross-sectional area of each TSV. I am working on algorithmic solutions to find the optimal number and placement of TSVs to deliver power in a 3D IC.