
Tufts University

School of Engineering
Department of Electrical and Computer Engineering

ES4 - Introduction to Digital Circuits

Spring 2007

Lab Section: Monday 4:30

Experiment 1

Introduction to breadboard prototypes

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PURPOSE

This lab was designed to make students more comfortable with the use of DIGI-DESIGNER breadboards, Very-High-Speed Integrated Circuit Hardware Description Language (VHDL), and the 7400 series of TTL logic gate integrated circuits. This involved an introduction to basic breadboard use and the Xilinx software package as well as an overview of the interior design of the TTL chips.

INTRODUCTION

Before wiring a circuit, it is important to note that sets of five nodes in each column of the breadboard are connected in series. To integrate a chip of 14 pins into a breadboard design, the chip should straddle the gap between sets of nodes so that pins 1 and 14, 2 and 13, 3 and 12, etc, are not in series.

The second important prerequisite for this lab was to familiarize oneself with the design of each 7400 series TTL integrated circuit (IC) utilized in the experiment. Notes on TTL IC design included which pins were for input and which were for output signals, and what type of logic gate each chip contained. The following table provides the appropriate information for each chip used. Diagrams of the chip input/output pins are included in the appendix of this report.

Table 1. TTL IC logic gates

CHIP	LOGIC GATES INCLUDED
7400	Two-input NAND
7402	Two-input NOR
7408	Two-input AND
7427	Three-input positive NOR
7432	Two-input OR

Once the structure of the ICs was understood, the programming environment presented in the Xilinx / ModelSim package had to be utilized. Xilinx is a VHDL editor that provides an environment in which to design and test logic circuits. ModelSim is a waveform generator that is used to simulate the testing of circuits, displaying the output from tested circuits timing diagrams.

Timing diagrams are graphs of the voltages of the input and output of a circuit over time. The square waves of these graphs can be thought of as representing logic 1 or true at the highest points, and logic 0 or false at the lowest points. Timing diagrams can be useful tools for the analysis of simple logic circuits, plotting the signals of inputs and outputs on the vertical axis and time on the horizontal.

MATERIALS

The following equipment and components were used:

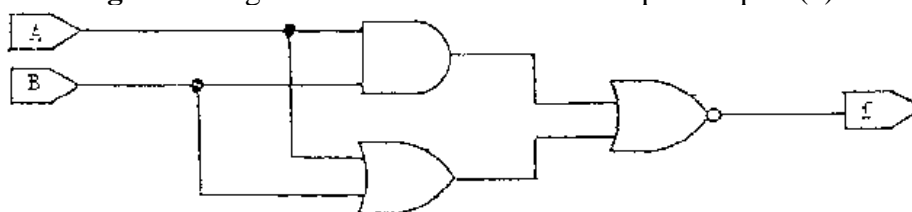
- DIGI-DESIGNER breadboard system (1)

- 1 each of:
 - 7400 TTL IC
 - 7402 TTL IC
 - 7408 TTL IC
 - 7427 TTL IC
 - 7432 TTL IC
- Oscilloscope
- Wire (varying lengths and colors)
- PC equipped with the following software:
 - ModelSim XE III 6.0a
 - Xilinx ISE 7.1i

PROCEDURE

The pre-lab assignment consisted of two parts: (a) to draw the wiring diagrams for utilization of one gate from each of the TTL chips (7400, 7402, 7408, 7427, 7432), and (b) to generate a wiring diagram for the logic diagram in Figure 1. The manufacturers data sheets (included in the Appendix) were used to identify the appropriate pins for input and output, as well as which type of gate was present in each chip.

Figure 1. Logic circuit to be constructed in pre-lab part (b).



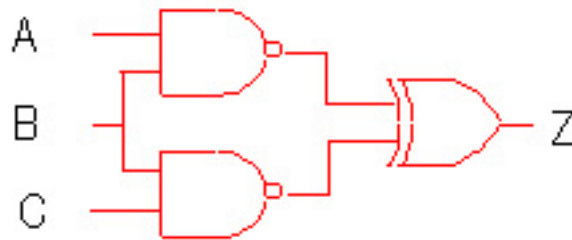
The first part of the in-lab project was to run a wire from a logic switch on the DIGI-DESIGNER breadboard to one of the lamps. Then the wire was taken from the logic switch and lamp and used to connect the oscilloscope to the J1 terminal on the breadboard. The oscilloscope was used to measure frequencies at different clock settings, including the 10 and 100 settings.

The wiring diagrams from the pre-lab part (a) were then used to construct the corresponding circuits on the breadboard. The logic switches were used as inputs, and the outputs were directed to the lamps which turned on or off to indicate logic 1 or logic 0, respectively. The logic switches were set to logic 1 and logic 0 in every possible combination, and the resulting output – indicated by the lamps – was recorded in a truth table. This was repeated for each chip.

The circuit of the wiring diagram in part (b) of the pre-lab was built on the breadboard, using the logic switches as inputs and a lamp as output. All possible combinations of input logic values were tested, and the results indicated by the lamps were recorded in a truth table. The truth table was used to identify the Boolean function of the circuit, which was recorded in the sum-of-products form.

The third section of the lab was devoted to VHDL. A truth table for the logic circuit in Figure 2 was made, and all eight combinations of A, B, and C (inputs) were used to determine the values of Z (output).

Figure 2. Logic circuit for Lab 1 Part 3:
 $Z = (AB)' \oplus (BC)'$



The circuit was modeled using the Xilinx and ModelSim software. To do this, NAND gate and XOR gate objects were created in Xilinx. The NAND was called twice, and the XOR once, from a separate structural entity that linked them all together to form the circuit in Figure 2. (The code for this section of the lab is included in the Appendix.)

ModelSim was used to run a simulation of the circuit built in Xilinx. A timing diagram was generated that illustrates the logic values of the components of the circuit for the different values of A, B, and C (inputs).

RESULTS

The wiring diagrams from pre-lab part (a) (and breadboard circuits constructed in-lab) are shown below. (The manufacturer's data sheets on each of these chips can be found in the Appendix.) A, B, and C represent inputs, and F represents output.

Figure 3. 7400 two-input NAND gate:

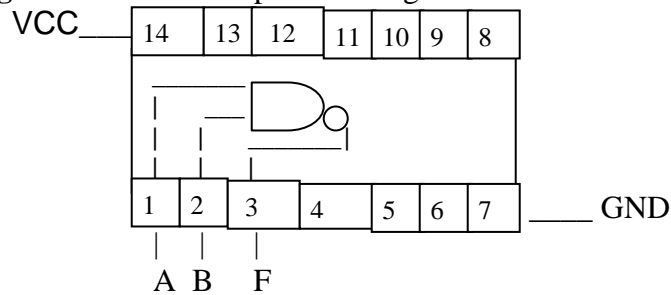


Figure 4. 7102 two-input NOR gate

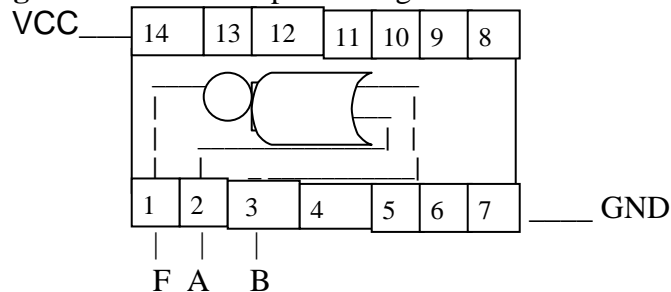
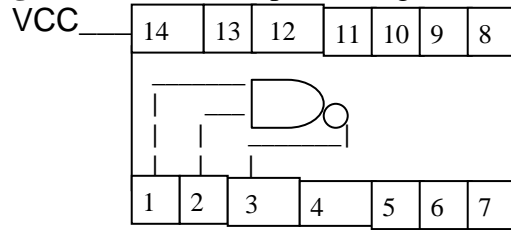
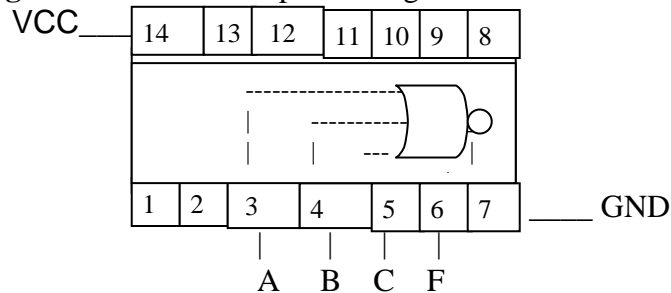
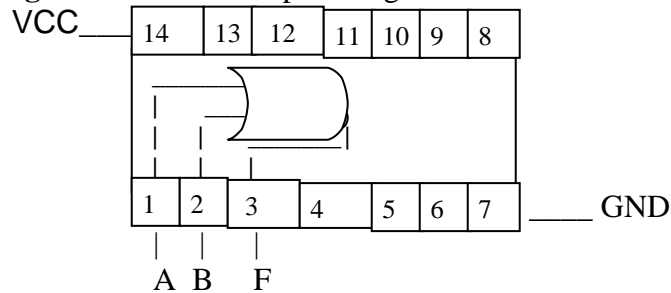


Figure 5. 7408 two-input AND gate**Figure 6.** 7427 three-input NOR gate**Figure 7.** 7432 two-input OR gate

When the logic switch was connected directly to the lamp, it was observed that turning the logic value of the switch to 1 turned the lamp on, while setting the logic value of the switch to 0 turned the lamp off, as described in Table 2.

Table 2. Relationship between logic switch and lamp

Value of logic switch	Lamp state
0	Off
1	On

When the oscilloscope was connected to the J1 terminal of the breadboard, the frequencies recorded were 10.17 Hz and 103.5 Hz for the 10 and 100 clock settings, respectively. Table 3 shows the range recorded for the intermediate values between the clock settings for x10 and x100.

Table 3. Frequency values for x10 and x100 clock settings

Clock setting	Frequency range (Hz)
X10	10.17 – 125.0
X100	103.5 - 1350

When the logic circuits from the pre-lab part (a) were wired on the breadboard, the outputs observed were recorded as in the following truth tables. A and B represent inputs, and F represents output.

Table 4. Truth table for 7400 two-input NAND

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

Table 5. Truth table for 7402 two-input NOR

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

Table 6. Truth table for 7408 two-input AND

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

Table 7. Truth table for 7427 three-input NOR

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Table 8. Truth table for 7432 two-input OR

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

The truth table for the logic circuit from part (b) of the pre-lab (see Figure 1) is provided in Table 9. The truth table shows that this logic circuit is equivalent to a NOR gate (the truth table for which is shown in Table 5). The function of the circuit can be expressed in sum-of-product form as: $F = A'B'$.

Table 9. Truth table for 7400 two-input NAND

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

For the third part of the lab, the logic circuit from Figure 2 was modeled and simulated. The code for the model consisted of two objects – a NAND and XOR gate – and a structural element that tied two NANDs and the XOR together to generate the desired circuit. Each object was coded as a structural “entity” with a simple function: The NAND gate took in a and b as two inputs, and applied it’s logic function with the line “x <= a nor b;” x being the output of the gate. The XOR was designed in a similar fashion, using the line “z <= x or y;” to apply the function of the gate. (For the XOR gate, x and y are input and z is output). The function that ties them all together does this by declaring two NAND components and one OR component, and creating busses between the components called temp1 and temp2. The calls to each gate were executed with the Port Map() function as follows:

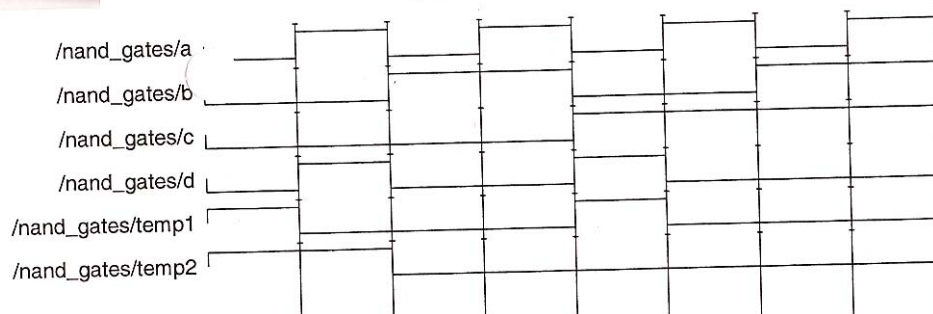
```
nand1: nand_gate
      Port Map (a, b, temp1);
nand2: nand_gate
      Port Map (b, c, temp2);
xor1: xor_gate
      Port Map (temp1, temp2, d);
```

The following outputs were determined for the eight possible combinations of input:

Table 10. Truth table for the circuit in Figure 2

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Figure 8 shows the timing diagram generated in ModelSim for Lab 1 Part 3.

Figure 8. Timing diagram of circuit in Figure 2.

CONCLUSION

This lab demonstrated how to use the lamps and logic switches to generate a truth table for a logic circuit. This can be more and more helpful as the complexity of the circuits analyzed increases. It also showed how to measure the frequency of a signal on the breadboard with the oscilloscope. The frequency ranges for x10 and x100 clock settings were not exactly 10-100 Hz and 100-1000 Hz, which could be useful information in future labs.

The lab also showed how Xilinx and ModelSim applications could be interfaced to produce a powerful tool for logic circuit analysis. With this tool, the truth table and timing diagram for the circuit from Part 3 of the lab (shown in Figure 2) were generated much more easily than they would have been by pencil and paper (once the experimenter learned how to use Xilinx and ModelSim, that is).

APPENDIX

Included in this section are the schematics for the interiors of the 7400 series TTL integrated circuits used in this lab, the pre-lab assignment (graded), the code written in Xilinx and the simulation results (printouts of output) corresponding to Lab 1 Part 3, and the loose-leaf sheets on which all data were recorded.